System and Method for Statistical Timing Analysis of Digital Circuits

ABSTRACT

The present invention is a system and method for statistical or probabilistic static timing analysis of digital circuits, taking into account statistical delay variations. The delay of each gate or wire is assumed to consist of a nominal portion, a correlated random portion that is parameterized by each of the sources of variation and an independent random portion. Arrival times and required arrival times are propagated as parameterized random variables while taking correlations into account. Both early mode and late mode timing are included; both combinational and sequential circuits are handled; static CMOS as well as dynamic logic families are accommodated. The timing analysis complexity is linear in the size of the graph and the number of sources of variation. The result is a timing report in which all timing quantities such as arrival times and slacks are reported as probability distributions in a parameterized form.